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Filed : **August 22, 2003**

REMARKS

In the December 15, 2004 Office Action, the Examiner rejects Claims 1, 2, 4, 8, 9, 12-14, 16, 17, 18, and 20 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,861,328 to Tehrani, et al. (Tehrani). The Examiner also rejects Claims 3, 5-7, 10, 11, 15, and 18 under 35 U.S.C. § 103(a) as being unpatentable over Tehrani in view of U.S. Patent No. 5,496,759 to Yue, et al., ("Yue"). Applicants respectfully traverse.

Discussion of Amendments to the Specification and Claims

The Examiner objected to the disclosure because of an informality in the priority information. Applicants have amended paragraph [0001] to recite "now U.S. Patent No. 6,623,987," have amended paragraph [0001] to update the status of a related application, also now issued, and accordingly request the Examiner to withdraw the objection to the informalities.

Discussion of Rejection of Independent Claim 1 Under 35 U.S.C. § 102(b)

The Examiner states that Figures 4-8 of Tehrani shows "all aspects of" the claimed invention. Applicants respectfully traverse. In particular, Applicants respectfully submit that Tehrani teaches two different processes, only one of which is illustrated in Tehrani's figures. Applicants submit that neither of Tehrani's two distinct processes teach or suggest the invention as claimed, and that there is no suggestion or motivation in Tehrani to modify the distinct processes in the manner recited by the Examiner. As will be explained in greater detail below, Applicants respectfully submit that Tehrani's first process does not teach or suggest a ***conductive*** etch stop barrier layer, and Tehrani's second process does not teach or suggest "encapsulating the top ***and side wall surfaces*** of a magneto-resistive bit with a conductive etch stop barrier layer" as claimed.

As explained in detail below, in rejecting Claim 1, the Examiner combines aspects of Tehrani's two distinct processes, thereby modifying the teachings of the Tehrani reference. Applicants respectfully submit that such a modification is not permissible in a rejection under 35 U.S.C. § 102(b).

> "The distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present. In other words, for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. Whereas, in a

rejection based on 35 U.S.C. 103, the reference teachings must somehow be modified in order to meet the claims. The modification must be one which would have been obvious to one of ordinary skill in the art at the time the invention was made. See MPEP § 2131 - § 2146 for guidance on patentability determinations under 35 U.S.C. 102 and 103."

See MPEP 706.02 IV. < DISTINCTION BETWEEN 35 U.S.C. 102 AND 103.

Because the Examiner is modifying the Tehrani reference, the appropriate statutory basis for rejecting Claim 1 can only be 35 U.S.C. § 103. "35 U.S.C. 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references." See MPEP 706.02(j). However, Applicants further note that "[e]ven when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2D 1313.

The Examiner's characterization of Tehrani is a modification of Tehrani. Figures 4-8 of Tehrani and, for example, Col. 5, lines 1-54 relate to the first process, and Col. 5 line 54 to Col. 6, line 13 relate to the second process.

Figure 6 illustrates forming of vias 47. Applicants note that vias 50 are not present in Figure 6, but rather, are formed later as shown in Figure 7. The forming of vias 47 and vias 50 in two different steps is a characteristic of the "first process," which is illustrated in Tehrani's figures. "***Subsequent*** to the patterning and etching of vias 47, via openings 50 are formed through dielectric cap 45," see Col. 5, lines 34-35 (emphasis added).

In describing the second process, Tehrani states that "[i]n a ***somewhat different process***, vias 47 and 50 are formed in a single operation," see Col. 5, lines 53-54 (emphasis added). Applicants note that this forming of vias 47 and 50 in a "single operation" is not illustrated by Figures 4-8, and submit that the Examiner is combining attributes of the figures, which relate to the first process, with incompatible attributes of the second process. Further evidence that two distinct processes is provided, "[a]fter the formation of vias 47 and 50, by either of the above described means," see Col. 6, lines 13-14. The distinction between the two processes of Tehrani is important because the processes and materials differ substantially between the two processes.

With respect to the first process, Tehrani teaches a "suitable barrier layer is, for example, silicon nitride," see Col. 5, lines 8-9 and a "suitable etch stop layer ... is, for example, AlO or

AlN," see Col. 5, lines 18-20. Accordingly, Applicants respectfully submit that Tehrani's first process does not teach or suggest a ***conductive*** etch stop barrier layer.

With respect to the second process, Tehrani states that "[t]he etch stop and passivation layer can be formed by using a material that is unreactive to oxide and silicon nitride RIE etches," see Col. 5, lines 65-66. It is in the context of the second process that Tehrani describes materials such as CrSi, see Col. 6, line 1. In this context, Tehrani further describes that "[v]ia opening 50 ***must be*** enclosed by GMR memory element 41, that is the contact ***may not extend outside the ends*** of GMR memory element 41 to protect element 41 from the resist stripping processes and other oxidizing or corrosive agents," see Col. 58-62.

Accordingly, the "etch stop and passivation layer" of Tehrani could not have been present "outside the ends of GMR memory element" in the second process, or the ends of element 41 would have been protected "from the resist stripping processes and other oxidizing or corrosive agents." Therefore, Applicants respectfully submit that, with respect to the second process of Tehrani, Tehrani does not teach or suggest "encapsulating the top ***and side wall surfaces*** of a magneto-resistive bit with a conductive etch stop barrier layer" as claimed.

Further, Applicants respectfully submit that certain aspects of the two distinct processes are not compatible with each other and cannot be interchanged. For example, a dielectric barrier is selectively removed, whereas a conductive layer can remain. For example, with respect to the dielectric barrier described with Tehrani's first process, Tehrani teaches that "[t]he barrier layer is removed with fluorine based chemistries, or other chemistries, which do not damage (oxidize or corrode) GMR element 41," see Col. 5, lines 48-50. By contrast, "where the etch stop and passivation layer is electrically conductive, contact metal (to be explained presently) can simply be deposited in contact ***therewith*** in vias 50," see Col. 6, lines 9-12 (emphasis added).

Therefore, Applicants respectfully submit that Tehrani does not teach or suggest Applicants' invention as defined by Claim 1, and Applicants request allowance of Claim 1.

Discussion of Rejection of Independent Claim 8 Under 35 U.S.C. § 102(b)

The Examiner rejects Claim 8 under 35 U.S.C. § 102(b) as being anticipated by Tehrani. In response, Applicants have amended Claim 8 to include that the etch stop barrier layer is conductive.

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As described in response to the Examiner's rejection of Claim 1, Applicants respectfully submit that with respect to Tehrani's second process, describing materials such as CrSi, the "etch stop and passivation layer" of Tehrani could not have been present "outside the ends of GMR memory element." Accordingly, Applicants respectfully submit that Tehrani does not teach or suggest "a conductive etch stop barrier layer that encapsulates the patterned GMR stack including the top surface ***and side walls*** of the GMR bit," as claimed.

Therefore, Applicants respectfully submit that Tehrani does not teach or suggest Applicants' invention as defined by Claim 8 as amended, and Applicants request allowance of amended Claim 8.

Discussion of Rejection of Independent Claim 12 Under 35 U.S.C. § 102(b)

The Examiner rejects Claim 12 under 35 U.S.C. § 102(b) as being anticipated by Tehrani. Applicants respectfully traverse.

As described in response to the Examiner's rejection of Claim 1, Applicants respectfully submit that with respect to Tehrani's second process, describing materials such as CrSi, the "etch stop and passivation layer" of Tehrani could not have been present "outside the ends of GMR memory element." Applicants respectfully submit that Tehrani does not teach or suggest "forming a conductive etch stop barrier layer over the substrate with the patterned magneto-resistive bit structure, the conductive etch stop barrier layer covering the top surface of the magneto-resistive bit structure ***and the side walls*** of the magneto-resistive bit structure," as claimed.

Therefore, Applicants respectfully submit that Tehrani does not teach or suggest Applicants' invention as defined by Claim 12, and Applicants request allowance of Claim 12.

Discussion of Rejection of Dependent Claims 3 and 15 Under 35 U.S.C. § 103(a)

The Examiner rejects Claims 3 and 15 under 35 U.S.C. § 103(a) as obvious over Tehrani in view of Yue. The Examiner acknowledges that Tehrani does not teach or suggest a thickness of the etch-stop layer.

Applicants respectfully submit that because Tehrani does not teach forming the conductive etch stop barrier layer on the side walls of a bit, a combination of Tehrani and Yue could not teach or suggest a thickness that would be appropriate for such a purpose. Further,

when applied to the side walls of a bit, a conductive etch stop layer is shunting, i.e., electrically in parallel with, the bit. This is described in paragraph [0024]. Also in paragraph [0024], Applicants described the desirability that the "shunting will be negligible."

Therefore, Applicants respectfully submit that the claimed thickness is not obvious over Tehrani in view of Yue. Accordingly, Applicants respectfully request the Examiner to withdraw the rejections to Claims 3 and 15, and to allow the same.

Discussion of Rejection of Other Dependent Claims

Dependent Claims 2, 4-7, 9-11, 13, 14, and 16-20 depend from and further define Claims 1, 8, or 12 (and/or intervening claims as applicable). The dependent claims recite numerous additional distinctions over the cited references.

In addition, Applicants respectfully submit that the rejections to dependent Claims 2, 4-7, 9-11, 13, 14, 16-20 are moot in light of the patentability of Claims 1, 8, or 12, and Applicants accordingly request allowance of Claims 2, 4-7, 9-11, 13, 14, and 16-20.

Summary

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner to withdraw the rejections of Claims 1-20 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a). Applicants further request the Examiner to allow Claims 1-20 and to pass the present application to the issue process.

If there is any further impediment to the prompt allowance of the present application, Applicants request the Examiner to call the undersigned attorney of record at 310-407-3466 or at the telephone number listed below to resolve any such impediment.

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Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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